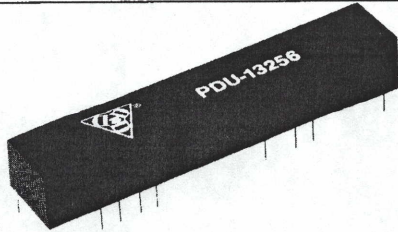


# Digitally Programmable Delay Units

**SERIES: PDU-13256**  
**(8 Bit) TTL Interfaced**



### Features:

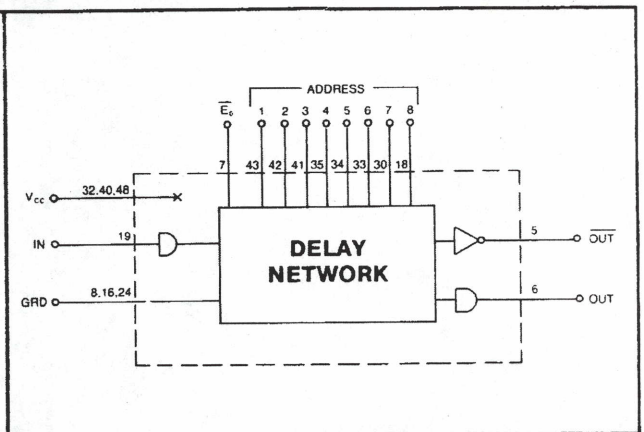
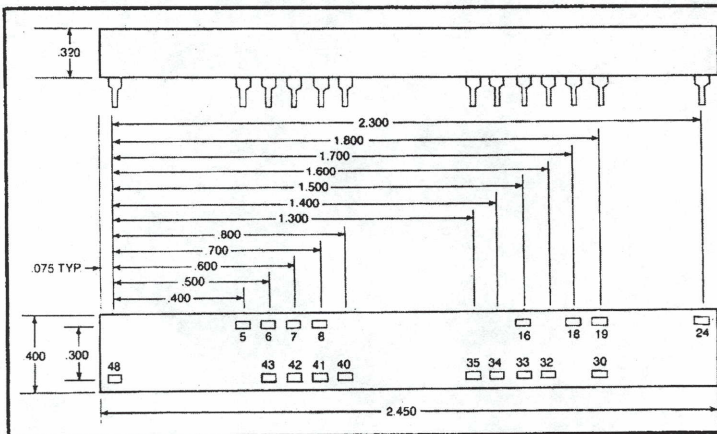
- Input & output TTL buffered
- 8-BIT TTL programmable delay line
- Two (2) separate outputs; inverting & non-inverting.
- Completely interfaced
- Compact & low profile

### Specifications:

- Input signal requirement: TTL logic
- Output fan-out: TTL schottky loads
- Delay variation: Monotonic in one direction
- Programmed delay tolerance:  $\pm 5\%$  or 2 NS whichever is greater
- Inherent delay ( $T_{D0}$ ): 44 NS on pin 6 } typical  
45 NS on pin 5 }
- Propagation delay:  
Address to output ( $T_{SUA}$ ) 12 NS typ.  
Enable to output ( $T_{SUE}$ ) 12 NS typ.
- Power dissipation: 1.1W Max.
- Supply voltage: 5 Vdc  $\pm 5\%$
- Operating temperature: 0-70 C
- Temperature Coefficient: 100 PPM/ C

### Test Conditions

- Input pulse-width:  $\sim 150\%$  of Max. delay.
- Input pulse spacing:  $\sim 3$  times of Max. delay.
- Input pulse voltage: TTL logic.
- Measurements taken @  $T_a = 25^\circ\text{C}$ ,  $V_{CC} = 5\text{V}$ .



TRUTH TABLE

Address (Bit No.)								Enable (E <sub>0</sub> )	Delay Out
8	7	6	5	4	3	2	1		
0	0	0	0	0	0	0	0	0	$T_0$
0	0	0	0	0	0	0	1	0	$T_1$
0	0	0	0	0	0	1	0	0	$T_2$
0	0	0	0	0	0	1	1	0	$T_3$
0	0	0	0	0	1	0	0	0	$T_4$
0	0	0	0	0	1	1	1	0	$T_7$
0	0	0	0	1	0	0	0	0	$T_8$
0	0	0	0	1	1	1	1	0	$T_{15}$
0	0	0	1	0	0	0	0	0	$T_{16}$
0	0	0	1	1	1	1	1	0	$T_{31}$
0	0	1	0	0	0	0	0	0	$T_{32}$
0	0	1	1	1	1	1	1	0	$T_{63}$
0	1	0	0	0	0	0	0	0	$T_{64}$
0	1	1	1	1	1	1	1	0	$T_{127}$
1	0	0	0	0	0	0	0	0	$T_{128}$
1	1	1	1	1	1	1	1	0	$T_{255}$
∅	∅	∅	∅	∅	∅	∅	∅	1	0

0 = Logic 0    1 = Logic 1    ∅ = Don't care.  
 $T_0$  = Reference or inherent delay of unit.  
 $T_1$  →  $T_{255}$  multiplier of incremental delay

Part No.	Incremental Delay Per Step	Total Programmed Delay NS
PDU-13256-5	.5 NS $\pm$ .3 NS	127.5
PDU-13256-1	1 NS $\pm$ .5 NS	255
PDU-13256-2	2 NS $\pm$ .5 NS	510
PDU-13256-3	3 NS $\pm$ 1.0 NS	765
PDU-13256-4	5 NS $\pm$ 1.0 NS	1,020
PDU-13256-5	5 NS $\pm$ 1.5 NS	1,275
PDU-13256-6	6 NS $\pm$ 1.5 NS	1,530
PDU-13256-7	7 NS $\pm$ 1.5 NS	1,785
PDU-13256-8	8 NS $\pm$ 2.0 NS	2,040
PDU-13256-9	9 NS $\pm$ 2.0 NS	2,295
PDU-13256-10	10 NS $\pm$ 2.0 NS	2,550

**NOTE:** 1. For the sake of simplicity all 256 programmable steps are not shown in this truth table.  
 2. After Bit 6, the incremental delay tolerance is 5% of programmed delay.